IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of forming a coupling dielectric in a memory cell comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming an oxide on a substrate;

forming Ta_2O_5 on the oxide;

oxidizing the Ta_2O_5 with rapid thermal process (RTP) at a temperature above the crystallization temperature for Ta_2O_5;

forming a cell nitride on the oxidized Ta_2O_5; [[and]]

forming a wetgate oxide on the cell nitride; and

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms.

2. (Original) The method of claim 1, wherein oxidizing the Ta_2O_5 with rapid thermal process (RTP) at the temperature above the crystallization temperature for Ta_2O_5 comprises:

oxidizing the Ta_2O_5 with rapid thermal process (RTP) in N_2O at a temperature of between about 750 degrees centigrade and about 900 degrees centigrade.

3. (Original) The method of claim 2, further comprising cooling for between about 55 seconds and about 65 seconds after oxidizing the Ta_2O_5.

4. (Withdrawn) A method of forming a coupling dielectric in a memory cell comprising:

forming an oxide on a substrate;

forming Ta_2O_5 on the oxide;

oxidizing the Ta_2O_5 with rapid thermal process (RTP) at a temperature below the crystallization temperature for Ta_2O_5;

forming a cell nitride on the oxidized Ta_2O_5; and

forming a wetgate oxide on the cell nitride.

5. (Withdrawn) The method of claim 4, wherein oxidizing the Ta_2O_5 with rapid thermal process (RTP) at the temperature below the crystallization temperature for Ta_2O_5 comprises:

oxidizing the Ta_2O_5 in rapid thermal process (RTP) in N_2O at a temperature of between about 400 degrees centigrade and about 725 degrees centigrade.

6. (Withdrawn) The method of claim 5, further comprising cooling for between about 55 seconds and about 65 seconds after oxidizing the Ta_2O_5.

7. (Currently Amended) A method of forming a coupling capacitor in a memory cell comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming an oxide on a substrate to a depth of about 30 angstroms;

forming a tantalum oxide having a crystallization temperature on the oxide to a depth of between about 60 angstroms and about 100 angstroms;

oxidizing the tantalum oxide at a temperature above the crystallization temperature of tantalum oxide;

forming a cell nitride on the oxidized tantalum oxide to a depth of between about 40 angstroms and about 60 angstroms; [[and]]

forming a wetgate oxide to a depth of between about 10 angstroms and about 50 angstroms on the cell nitride; and

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms.

8. (Original) The method of claim 7, wherein forming the tantalum oxide on the oxide to the depth of between about 60 angstroms and about 100 angstroms comprises:

forming Ta_2O_5 on the oxide to a depth of between about 60 angstroms and about 100 angstroms.

9. (Original) The method of claim 8, further comprising oxidizing the tantalum oxide in rapid thermal processing (RTP) in N_2O for about 60 seconds.

10. (Withdrawn) A method of forming a coupling capacitor in a memory cell comprising:

forming an oxide on a substrate to a depth of about 30 angstroms;

forming a tantalum oxide having a crystallization temperature on the oxide to a depth of between about 60 and about 100 angstroms;

oxidizing the tantalum oxide at a temperature below the crystallization temperature of tantalum oxide;

forming a cell nitride on the oxidized tantalum oxide to a depth of between about 40 angstroms and about 60 angstroms; and

forming a wetgate oxide to a depth of between about 10 angstroms and about 50 angstroms on the cell nitride.

11. (Withdrawn) The method of claim 10, wherein forming the tantalum oxide on the oxide to the depth of between about 60 and about 100 angstroms comprises:

forming Ta_2O_5 on the oxide to a depth of between about 60 angstroms and about 100 angstroms.

12. (Withdrawn) The method of claim 11, further comprising oxidizing the tantalum oxide in rapid thermal processing (RTP) in N_2O for about 60 seconds.

13. (Currently Amended) A method of forming a coupling dielectric in a memory cell comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming a layer of SiO_2 on a substrate;

forming a layer of Ta_2O_5 on the layer of SiO_2;

forming a layer of Si_3N_4 on the layer of Ta_2O_5; [[and]]

forming a wetgate oxide layer of SiO_2 on the layer of Si_3N_4;

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms; and

forming the dielectric stack to have a capacitance of at least 25% greater than an oxide-nitride-oxide insulator having a thickness of between 140 angstroms and 240 angstroms.

14. (Original) The method of claim 13, wherein forming the layer of SiO_2 on the substrate comprises forming the layer of SiO_2 on germanium.

15. (Currently Amended) The method of claim 14, wherein forming the layer of Ta_2O_5 on the layer of SiO_2 comprises oxidizing the tantalum oxide layer above the crystallization temperature.

16. (Currently Amended) A method of forming a coupling dielectric in a memory cell, comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming an oxide layer on a substrate;

forming a tantalum oxide layer on the oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a wetgate oxide layer on the nitride layer such that the dielectric stack has a thickness of between 140 angstroms and 240 angstroms;

17. (Original) The method of claim 16, wherein forming the oxide layer on the substrate comprises forming the oxide layer on gallium arsenide.

18. (Currently Amended) The method of claim 16, wherein forming the tantalum oxide layer on the oxide layer comprises oxidizing the tantalum oxide layer above the crystallization temperature.

19. (Currently Amended) A method of forming a coupling dielectric in a memory cell, comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming a thermally grown oxide layer having a thickness of between about 28 angstroms and about 32 angstroms on a substrate;

forming a tantalum oxide layer on the thermally grown oxide layer;

forming a nitride layer on the tantalum oxide layer; [[and]]

forming a wetgate oxide layer on the nitride layer; and

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms.

20. (Original) The method of claim 19, wherein forming the thermally grown oxide layer having a thickness of between about 28 angstroms and about 32 angstroms on the substrate comprises forming the thermally grown oxide layer on a silicon-on-sapphire substrate.

21. (Currently Amended) The method of claim 19, wherein forming the tantalum oxide layer on the thermally grown oxide layer comprises reoxidizing the tantalum oxide layer by rapid thermal processing.

22. (Currently Amended) A method of forming a coupling dielectric in a memory cell, comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming an oxide layer on a substrate;

forming a tantalum oxide layer by metal organic chemical vaport deposition to a thickness of beween about 60 angstroms and about 100 angstroms on the oxide layer;

forming a nitride layer on the tantalum oxide layer; [[and]]

forming a wetgate oxide layer on the nitride layer; and

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms.

23. (Original) The method of claim 22, wherein forming the oxide layer on the substrate comprises forming the oxide layer on an amorphous material.

24. (Original) The method of claim 22, wherein forming the oxide layer on the substrate comprises forming the oxide layer by chemical vapor deposition.

25. (Currently Amended) A method of forming a coupling dielectric in a memory cell, comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming an oxide layer on a substrate;

forming a layer of a material having a permittivity of between about ten and about twelve on the oxide layer;

forming a nitride layer on the tantalum oxide layer; [[and]]

forming a wetgate oxide layer on the nitride layer; and

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms.

26. (Original) The method of claim 25, wherein forming the oxide layer on the substrate comprisies forming the oxide layer on a n+ substrate.

27. (Original) The method of claim 25, wherein forming the oxide layer on the substrate comprises forming the oxide layer by chemical vapor deposition.

28. (Currently Amended) A method of forming a coupling dielectric in a memory cell, comprising:

forming a dielectric stack, wherein forming the dielectric stack includes:

forming an oxide layer on a substrate;

forming a tantalum oxide layer on the oxide layer;

forming a nitride layer having a thickness of between about 40 angstroms and about 60 angstroms on the tantalum oxide layer; [[and]]

forming a wetgate oxide layer on the nitride layer; and

forming the dielectric stack to a thickness of between 140 angstroms and 240 angstroms.

29. (Original) The method of claim 28, wherein forming the oxide layer on the substrate comprises forming the oxide layer on a germanium substrate.

30. (Original) The method of claim 28, whereon forming the nitride layer having the thickness of between about 40 angstroms and about 60 angstroms on the tantalum oxide layer comprises forming the nitride layer by low pressure chemical vapor deposition.

31. (Currently Amended) A method of forming a coupling dielectric in a memory cell, comprising:

forming a dielectric stack to a thickness of between 140 angstroms and 240 angstroms, wherein forming the dielectric stack includes:

forming an oxide layer on a substrate;

forming a tantalum oxide layer on the oxide layer;

forming a nitride layer on the tantalum oxide layer; and

forming a wetgate oxide layer having a thickness of between about 10 angstroms and about 50 angstroms on the nitride layer.

32. (Original) The method of claim 31, wherein forming the oxide layer on the substrate comprises forming the oxide layer on a silicon substrate.

33. (Original) The method of claim 31, wherein forming the oxide layer on the subsrate comprises forming the oxide layer on a gallium arsenide substrate.

34. (New) The method of claim 1, wherein forming the dielectric stack comprises forming the dielectric stack to have a capacitance of at least 25% greater than an oxide-nitride-oxide insulator having a thickness of between 140 angstroms and 240 angstroms.

35. (New) The method of claim 7, wherein forming the dielectric stack comprises forming the dielectric stack to have a capacitance of at least 25% greater than an oxide-nitride-oxide insulator having a similar thickness compared to the dielectric stack.

36. (New) The method of claim 16, wherein forming the dielectric stack comprises forming the dielectric stack having a capacitance of 25% to 35% greater than an oxide-nitride-oxide insulator with a thickness of between 140 angstroms and 240 angstroms.

37. (New) The method of claim 19, wherein the dielectric stack has a capacitance of at least 25% greater than an oxide-nitride-oxide insulator having a thickness of between 140 angstroms and 240 angstroms.

38. (New) The method of claim 22, wherein forming the dielectric stack providing a capacitance for the dielectric stack of 25% to 35% more when compared to an oxide-nitride-oxide insulator having a thickness of between 140 angstroms and 240 angstroms.

39. (New) The method of claim 25, wherein forming the dielectric stack has a capacitance of the dielectric stack of at least 25% greater than an oxide-nitride-oxide insulator having a thickness of between 140 angstroms and 240 angstroms.

40. (New) The method of claim 28, wherein the dielectric stack is formed to exhibits much more capacitance compared to an oxide-nitride-oxide insulator having similar thickness.

41. (New) The method of claim 31, wherein forming the dielectric stack has a capacitance value of 25% to 35% larger than an oxide-nitride-oxide insulator with the substantially similar thickness.